CréVinn

CréVinn provides Silicon Design Services for the Networking, Computing, Automotive and general Digital Electronics markets.

CréVinn also develops high-performance IP cores to complement our Design Service business, focused on the high-performance networking field.

CréVinn's key skill is in combining intelligence in silicon with a proven track record in simplifying complex technology. The result is a high-function design at optimum cost, delivered to our customers with short yet predictable schedules.

Company Profile

CréVinn was founded May 2002 with a core ASIC design team from 3Com's Silicon Design Group.

The team has been instrumental in the development of many pioneering ASICs and IP cores for market-leading products in the last decade. These cover a wide range of networking and computing applications such as Layer 2/3/4 Switches, Gigabit and 10 Gigabit Ethernet Controllers, Hardware Accelerators for Network Processing tasks, Encryption and Wireless cores, High Speed Interprocessor Switches, Audio/Video over Networks, Automotive and Industrial SoCs.

Since our foundation we have grown steadily, now with two design centres – Galway and Dublin, Ireland, serving the networking, computing, automotive and industrial markets.

Galway Design Centre

Dublin Design Centre

Design Services

Consultancy :

With over 20 years experience in Architecture, Design and Implementation of ASICs and FPGAs, one of CréVinn's key strengths is the ability to participate with customers in the product definition and architectural phases of ASIC-based systems.

With our background in the development of high functionality silicon-based products we can help you identify the key features and tradeoffs needed to optimise your products for the market.

Silicon Design / Verification Services :

In addition to consultancy expertise, CréVinn is fully resourced to implement your ASIC or FPGA Design and/or Verification project.

For ASICs, our team - experienced in developing some 30+ chips with the major ASIC vendors - has the proven ability to bring your design successfully from Architectural stages through to the completed device.

Fletcher ASIC Design activity at CréVinn

For FPGAs, CréVinn brings its strength in structured ASIC design methodology to the FPGA world. We adopt the same meticulous approach to FPGA design that has brought us first pass success with ASICs, ensuring that your designs reach the market with the same high quality levels, whether ASIC or FPGA. In the area of Verification, we adopt the latest VMM-based methodology where appropriate, delivering a comprehensive constrained-random self-checking verification suite on project completion.

Engaging with CréVinn :

The preferred engagement model is a fully-costed service for the project. We work closely with customers to assess project costs and schedule before start-up.

Projects therefore begin with an agreed Statement of Work, a fixed fee and a defined schedule. Most of our customers find this approach beneficial in that it removes uncertainty in project schedule and costs.

CréVinn also operates other models such as development on a time and materials basis, development with split fees and royalties, and other models – tailored to the needs our customers.

Along with our service business, CréVinn is building a portfolio of IP (Intellectual Property) cores. CréVinn can offer this IP to customers directly, or as part of a bundled package covering both Design Services and IP.

CréVinn Teoranta : Baile an tSagairt, Spiddal, Co. Galway, IRELAND;
Phone +353-91-558090 Fax: +353-91-558060

E8 Calmount Business Park, Calmount Rd., Ballymount, Dublin 12, IRELAND
Phone +353-1-4604754 Fax: +353-1-4060208

IP Cores

Current trends in networking have expanded the role of the network interface to include complex functionality - technologies such as Secure Communications, Traffic Management and Network Storage.
In parallel network line speeds have continued to increase, with Gigabit Ethernet now pervasive and 10 Gigabit products gaining ground in the market. The combination of complexity and speed has driven the need to move much of this functionality into specialised processing units in the network interface.

Many of today's implementations are based on the use of fully programmable Network Processors, which are ideal for solving generic data handling problems. This flexibility comes at a price - in silicon area, firmware development and scalability.

For many applications, this flexibility is not required - although the complexity still often drives the use of fully programmable network processors. The TCP protocol for example, which can require 15,000 lines of code for a standard implementation, is complex but well defined.

CréVinn's approach is to implement such protocols using configurable Hardware State Machines. This approach allows customers to tailor cores to their particular requirements while removing the firmware development cycle, yielding the best of both worlds - minimised silicon area with an appropriate level of programmability.

Our cores are developed as 'Soft Macros', making integration with our customers' target technologies a painless experience. In addition the 'soft macro' approach facilitates scaling to suit different performance requirements.

In particular, we are happy to tailor IP Cores to suit individual customer applications.

ASIC/Core design experience

The following table lists a selection of the chips and IP Cores developed by the team in recent years.

Typically the team worked closely with the end customer to define the overall product requirements, leading on to identifying opportunities for ASICs or FPGAs such as those in the table, to achieve aggressive cost and performance goals. Following this, chip specifications to meet these goals were produced, and wherever feasible, IP Cores specified within such ASICs aimed at maximising reuse opportunities across many applications.

Often, a ground-breaking ASIC or Core became the founder member of a follow-on family of ASICs for parallel markets, or future generations of the original product.

CréVinn is currently developing second and third generations of a number of chip-sets for customers in the networking and automotive industries.

Our design experience as a team covers many areas within the Networking field, along with several developments in the Computing and Automotive/Industrial fields.

Areas of expertise include technologies such as :

- Ethernet switching and it's many associated fields - Layer2 switching, Layer 3 switching, QoS and VLANs (802.1p,q), 802.3x flow-control, RMON I and II, amongst others
- Packet Analysis techniques, such as search engines (hash-based, trie-based, binary tree and so on) for IP packet forwarding lookup, packet classification for flow-identification, or deep packet inspection for security applications
- Traffic analysis - rate monitoring and precise rate control of traffic flows, based on various classification parameters
- TCP/IP protocol in silicon – full TCP/IP communications in hardware state-machines, for low-overhead communications (TOE), applications such as security (stateful packet inspection), and transporting low-latency video over LAN and WAN networks
- Techniques for automotive, industrial and general electronics fields, such as LIN bus, DSP techniques (Correlators, Filters), Quadrature encoders, PWM control interfaces, DDR I and II memory controllers, RLDRAM, QDR, ECC, Flash controllers
- System-on-Chip techniques, such as embedded CPUs (Arm, 8051, Mips, DSP processors), AMBA buses, high-speed/low-latency on-chip communications between IP cores, low-power techniques, design/integration of many cores such as USB, 1394, xVGA displays, I^2C, SMBUS, Uarts, Timers, Keyboard i/o, Bluetooth, 802.11 a/b/g, Encryption (AES, (3)DES, SHA)
- Soft macro CPU design, including configurable architectures and custom instructions to suit particular applications

Chips	Description	Features
A	10 Mbps Layer2 Switch chip	Low-cost 10M and 100M switching silicon
B	4x10, 1x100 Ethernet MAC	Fast Ethernet, IFM (pre 802.3x), TDM bus
C	ATM-Ethernet/Token-ring i/f	LANE in hardware, switch downlink
D	Gigabit MAC ASIC	Gigabit Mac core reused in many other ASICs
E	10/100 Mbps Switch ASIC	Added RMON 1,2 hw accelerators
F	4x10/100 Mac chip	Dynamic Tx buffers, 802.1x
G	12x10/100 Mac chip	(as above)
H	Gigabit downlink single-chip ASIC	First Gigabit MAC implementation
I	Quad Gigabit downlink, cascade ASIC	Quad embedded Serdes, distributed cascade arbitration protocol
J	10Gig proprietary Ethernet MAC	Pre-standard chassis backplane application
K	4-port Gigabit Switch ASIC	LVDS hi-speed "matrix" bus, Layer 3 switching
L	SoC (System-on-Chip) ASIC, integrating many cores	SoC Arch, IP Core integration, (Risc, DSP, USB, 1394, L2 Switch etc), IPSec (3DES, SHA-1,MD5)
P	CPU switch ASIC	Multiple 64-bit CPU switching, Strong RAS (Reliability, Availability, Serviceability), DDR DRAM ctrl, multi-phase PLL, ECC, Pin-steering
Q	4 million pkt/sec traffic analyser/rate-controller	2 GBit Ethernet traffic analyser, precise rate control (4m flows)
R	Mixed signal automotive chip	Mini-SoC, 8051-based, ultrasonic stimulus/sensors, with DSP features such as correlation functions
S	Networked Digital Video chip	1Gbit/sec Ethernet low-latency networked video chip with in-built TOE
T	15 million pkt/sec traffic analyser/rate-controller	10 GBit Ethernet traffic analyser, precise rate control (16m flows)
U	Mixed signal industrial chip	SoC, ARM-based, control applications (Pulse-width modulation, Quadrature Encoding), low-power features
V	Mixed signal automotive chip	SoC, ARM-based, general-purpose automotive applications (LIN, SPI, I2C, async comms, timers, power-down modes etc.)
W	Mixed signal automotive chip	Mixed-signal sensor chip for automotive and industrial applications, including digital filters (Sigma-Delta)

Cores	Description	Features
a	802.11 a/b/g core	DSP (OFDM, PLCP, Mac), SoC cores, Encryption (RC4, AES)
b	10G Ethernet Mac core	Fully IEEE 802.3ae compliant
c	10G PCS core (10GBaseX)	10GBaseX PCS compliant with IEEE 802.3ae D5.0 May 1 2002 Clause 48 specifications
d	Search Engine	CAM-style, wire-speed content analysis of Gigabit-speed network traffic, ISP applications
e	1G TCP Offload Engine	1Gbps, low-cost on-chip connection tables/external DDR DRAM
f	10G TCP Offload Engine	10Gbps,as above, under development
g	High Performance Search Engine	CAM-style, wire-speed content analysis of 10 Gigabit-speed network traffic, ISP applications

Recent ASICs, Cores developed by the team

CréVinn Teoranta : Baile an tSagairt, Spiddal, Co. Galway, IRELAND;
Phone +353-91-558090 Fax: +353-91-558060

E8 Calmount Business Park, Calmount Rd., Ballymount, Dublin 12, IRELAND
Phone +353-1-4604754 Fax: +353-1-4060208

Development Process

CréVinn's Development Environment has been developed over many years of ASIC and FPGA design.

Key to the architectural and design stages is the Fletcher Design Methodology. Amongst its many benefits, the methodology leads to naturally self-documenting designs.

Backing this up is a comprehensive set of well-honed ASIC/FPGA Development Procedures. In addition, each project generates a set of project-specific documents based on standard templates, such as Functional Specifications and Verification Plans.

Referring to the Development Environment diagram, CréVinn can engage with customers at any point.

When engaging at the Concepts and Architectural Design stages, the ASIC/FPGA requirements are typically determined during joint white-boarding sessions at the customer site.

When beginning an engagement after the architectural stage, CréVinn can translate customer's architectural specifications or outline functional requirements into detailed ASIC Functional Specifications, for review and agreement before initiating detailed designs.

In the above engagement examples, the Fletcher methodology is an ideal mechanism to accelerate a new design through its architectural and design stages, either with a CréVinn design team only, or as a joint development.

We also have the flexibility of initiating an engagement during the Detailed Design stage, for example in the case of upgrading an existing customer design. The Fletcher methodology is also very beneficial here, in clearly delineating the existing and new functions, leading to a well-integrated upgraded design.

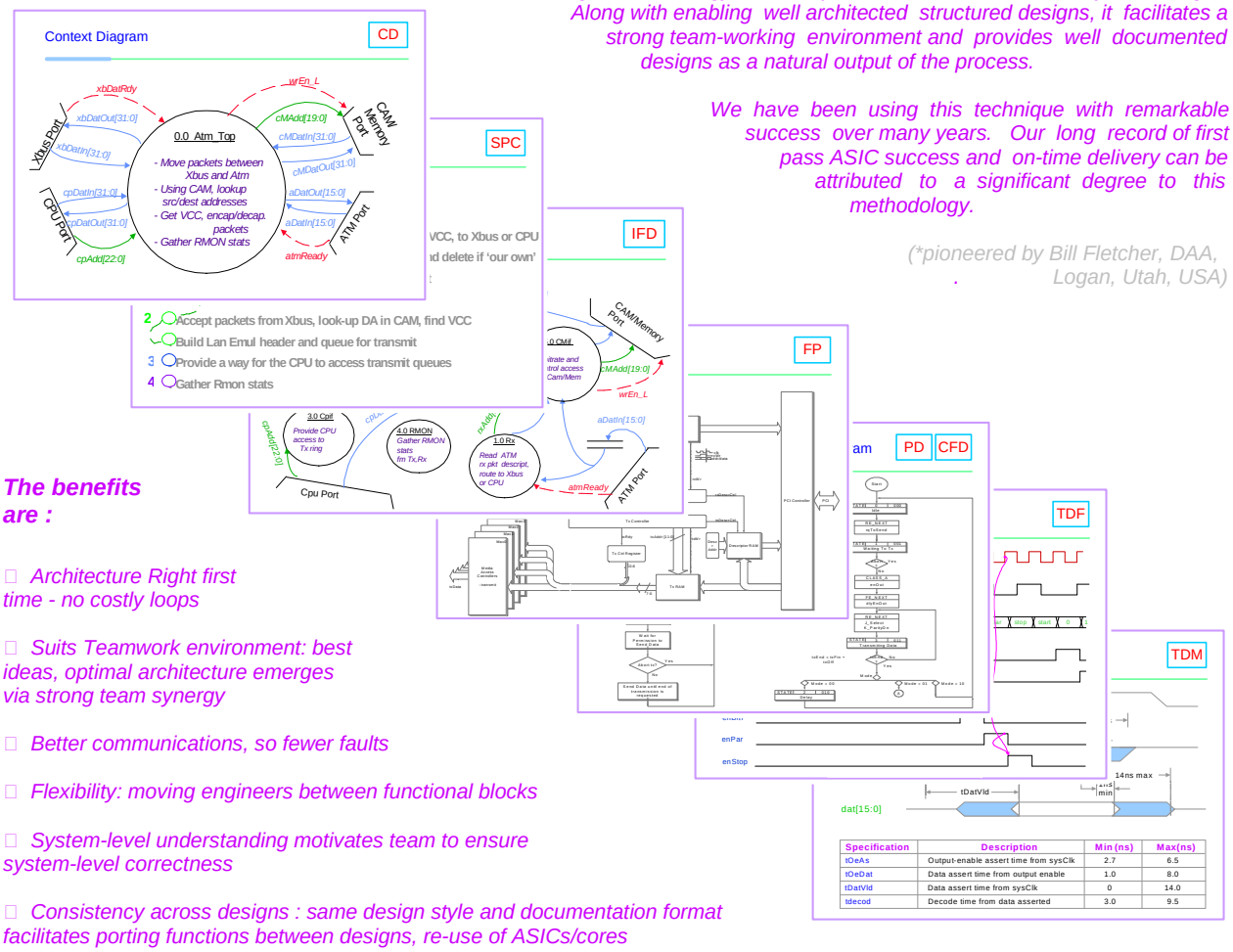
CréVinn typically works closely with customers / ASIC vendors at the Physical Implementation state, often on-site. CréVinn may also begin an engagement with customers during this stage, where our experience in physical design issues can be applied to the challenges involved with synthesis, timing closure, floor-planning, scan insertion, vector generation and other back-end tasks leading to a successful tape-out.

Structured Design Methodology

CréVinn uses a structured top-down design approach called the "Fletcher Design Methodology", which provides us with several key advantages. Along with enabling well architected structured designs, it facilitates a strong team-working environment and provides well documented designs as a natural output of the process.*

We have been using this technique with remarkable success over many years. Our long record of first pass ASIC success and on-time delivery can be attributed to a significant degree to this methodology.

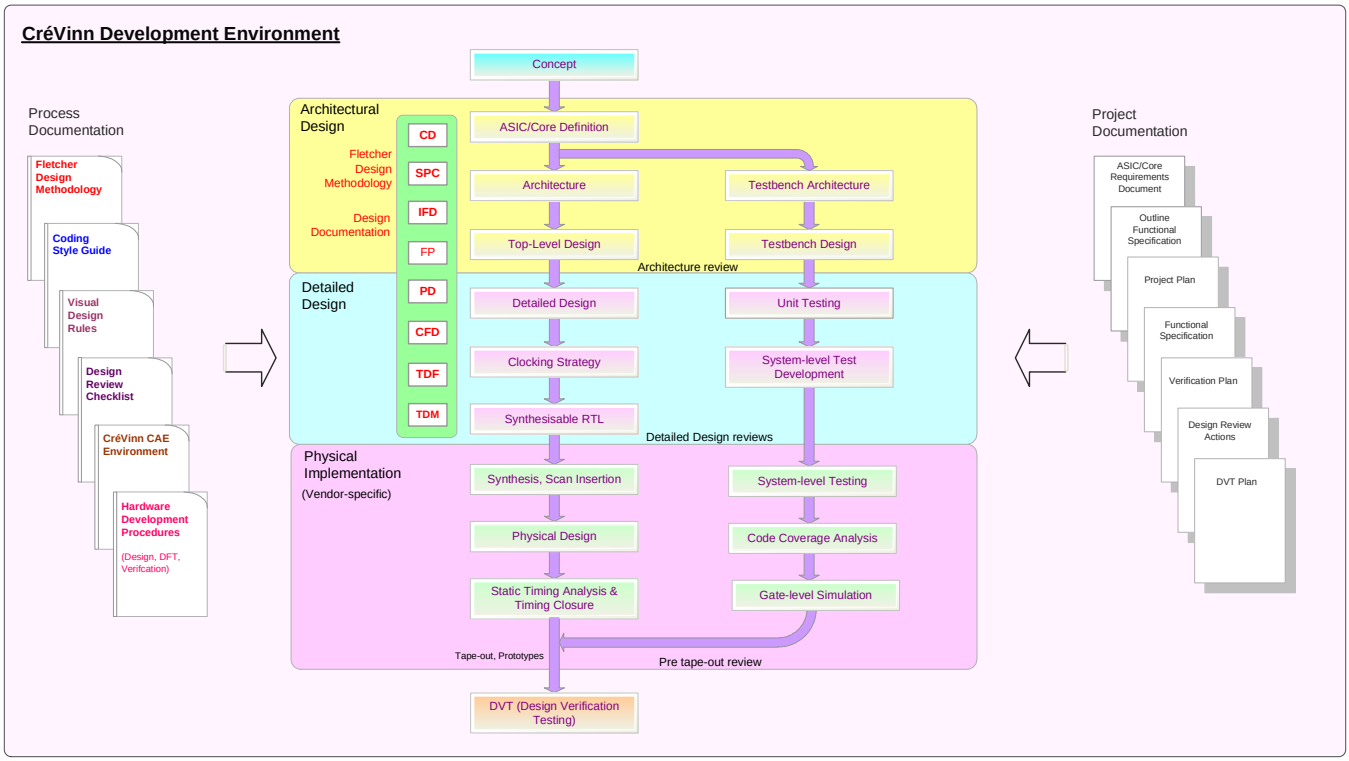
*(*pioneered by Bill Fletcher, DAA, Logan, Utah, USA)*



Specification	Description	Min (ns)	Max(ns)
tOeAs	Output-enable assert time from sysClk	2.7	6.5
tOeDat	Data assert time from output enable	1.0	8.0
tDatVld	Data assert time from sysClk	0	14.0
tdecod	Decode time from data asserted	3.0	9.5

The benefits are :

- *Architecture Right first time - no costly loops*
- *Suits Teamwork environment: best ideas, optimal architecture emerges via strong team synergy*
- *Better communications, so fewer faults*
- *Flexibility: moving engineers between functional blocks*
- *System-level understanding motivates team to ensure system-level correctness*
- *Consistency across designs : same design style and documentation format facilitates porting functions between designs, re-use of ASICs/cores*



Verification Methodology

A key part of the Development Process is the Verification Methodology. The testbench diagram shows a number of techniques we use depending on the project needs, such as :

- Cycle-accurate models, appropriate for deterministic designs; independently developed models, written for example in RTL or System-C, compare with the RTL/gate-level "DUT" (device under test) on a per-cycle basis, instantly flagging unexpected behaviour.
- High-level behavioural models (written using C, Vera or equivalent, System Verilog, or regular RTL), appropriate for complex functions which are deterministic on a deeper basis, such as a "per-packet" basis - not per clock cycle.
- Extensive use of VMM/OVM/UVM-based verification elements. Rapid Testbench creation via CréVinn's library of base-classes extended for a wide variety of applications in the area of Networking and SoCs.
- Testbench using System Verilog, Native Testbench (VCS), or Verilog/VHDL
- Assertion points, some buried in the design, some on the external buses, are used to check for violations of specifications, protocols etc. These can be removed prior to final RTL, or remain in the design and coupled to a "visibility bus" or "visibility registers" for use in prototype verification.
- A "Random Stimulus Generator", constrained for various test scenarios, is used as a stimulus source, backed up with a suite of directed tests where appropriate. Functional coverage "bins" buried in the design (but not in final RTL) guide the Random Stimulus Generator to achieve greater coverage.

Comprehensive self-checking tests based on the above techniques are developed during the project, using a combination of random and directed tests.

Both functional-oriented and stress-oriented test suites are created, with the end result being not just a fully verified design, but also a comprehensive "Regression Test Suite" for use both during the latter stages of the project, and for future design upgrades.